

# Spartan LLRF for ILC

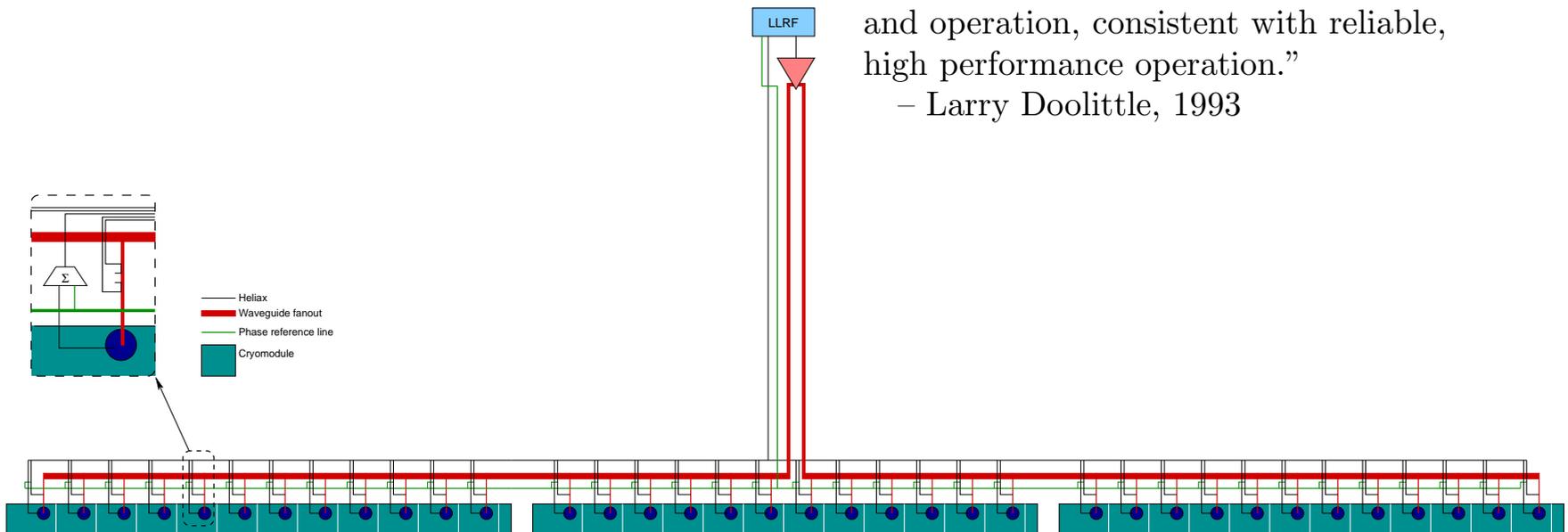
Larry Doolittle, LBNL

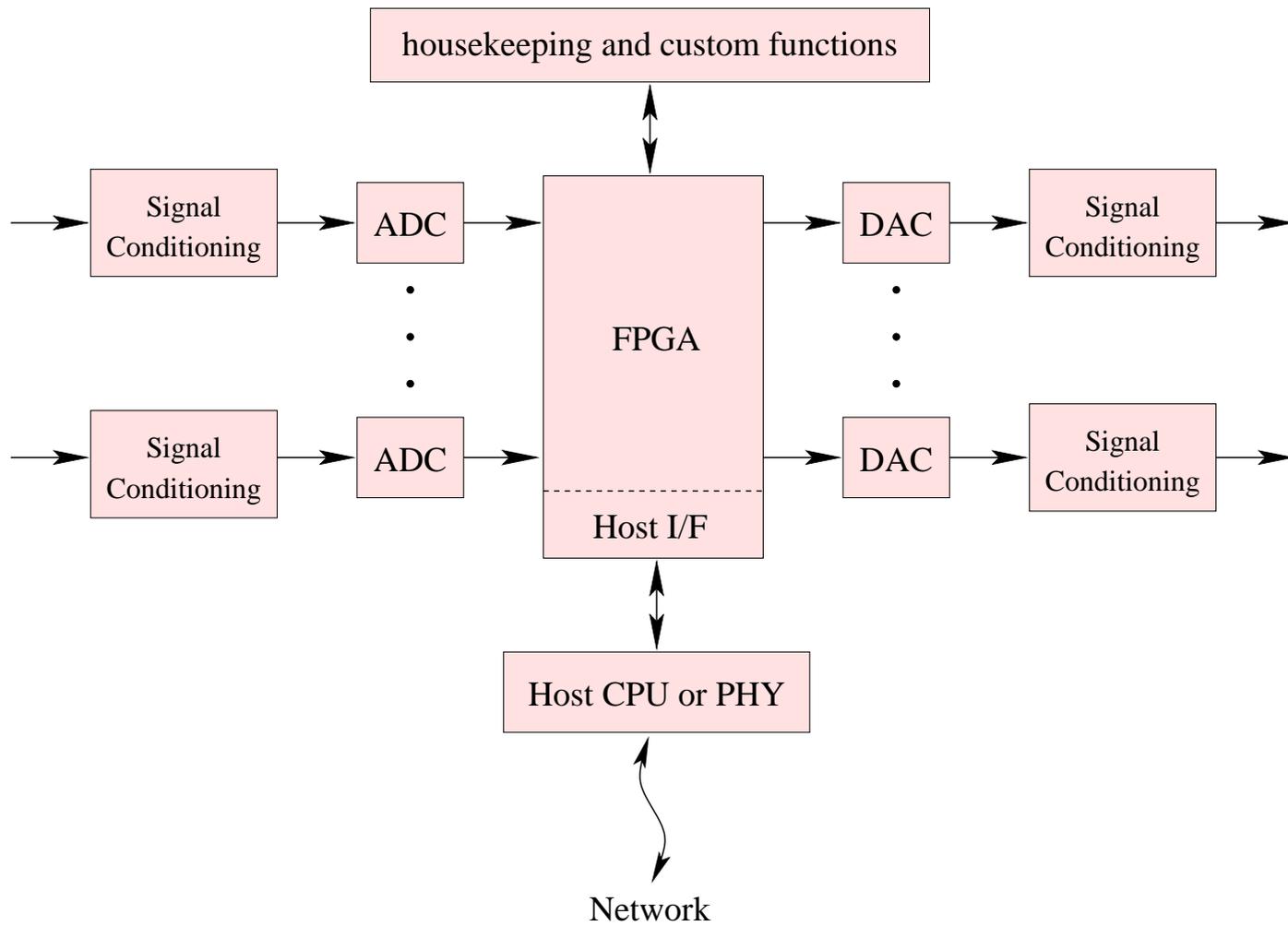
WG1 of LLRF07, Knoxville, October 2007

- Outline of problem to be solved
- LLRF4 board to evaluate concepts
- Topics needing further work

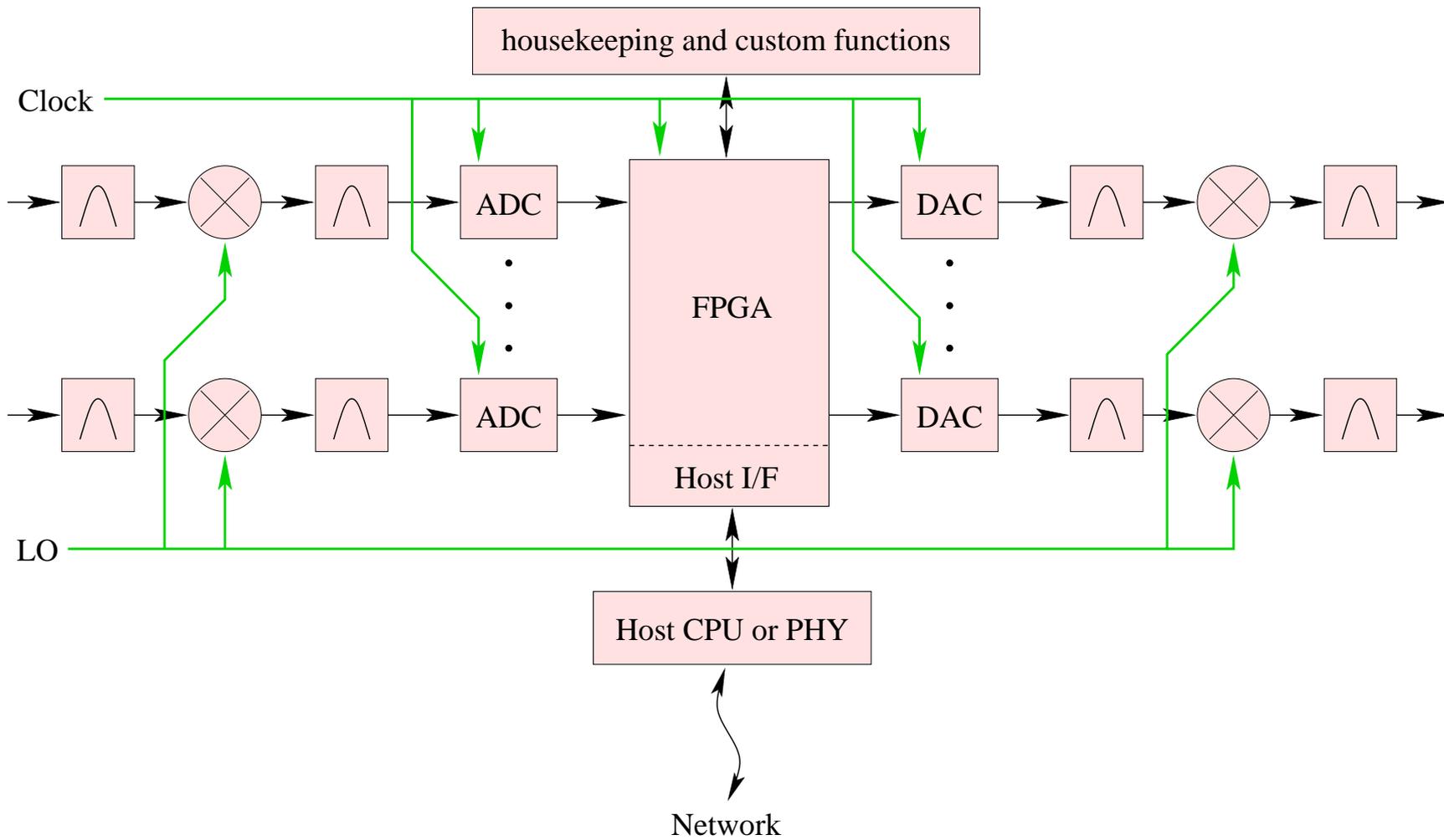
“System should be designed for the lowest possible cost, including installation and operation, consistent with reliable, high performance operation.”

– Larry Doolittle, 1993

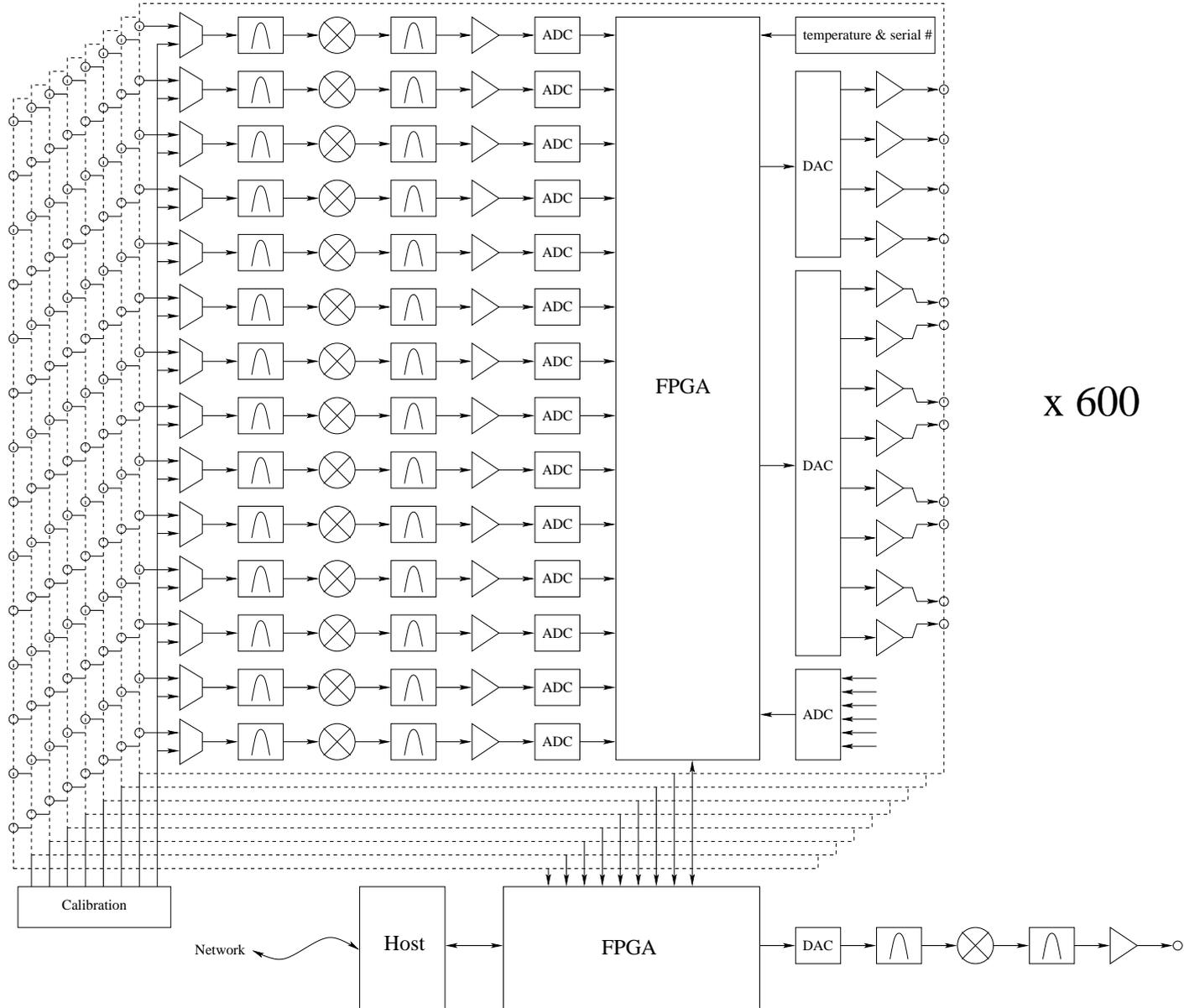




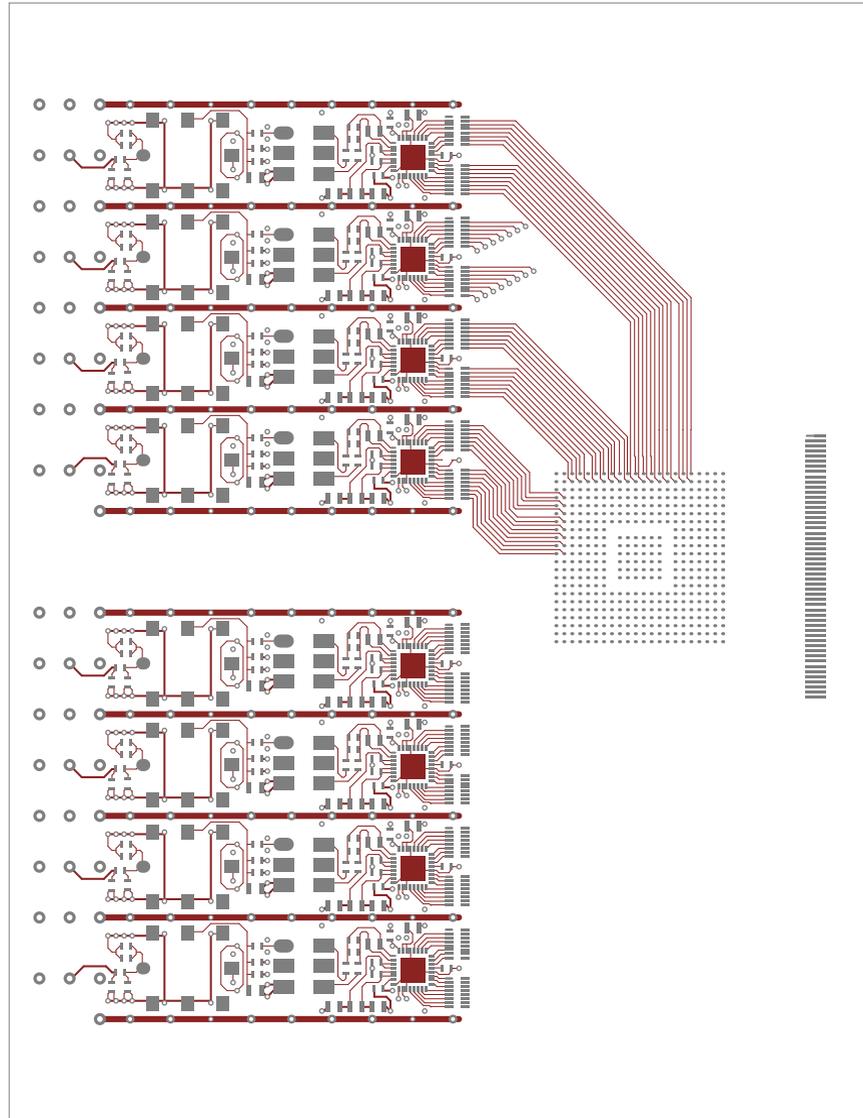
Familiar block diagram



Familiar block diagram, with RF signal conditioning



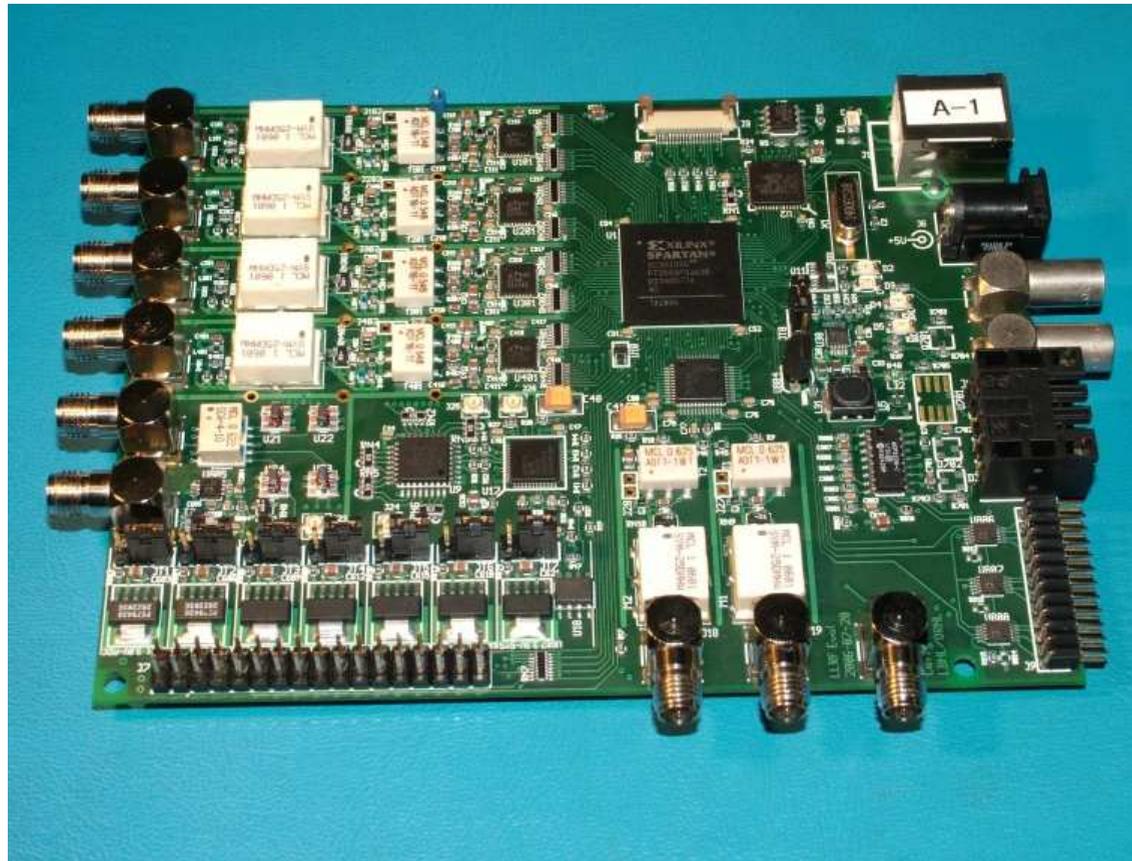
Familiar block diagram, scaled for ILC



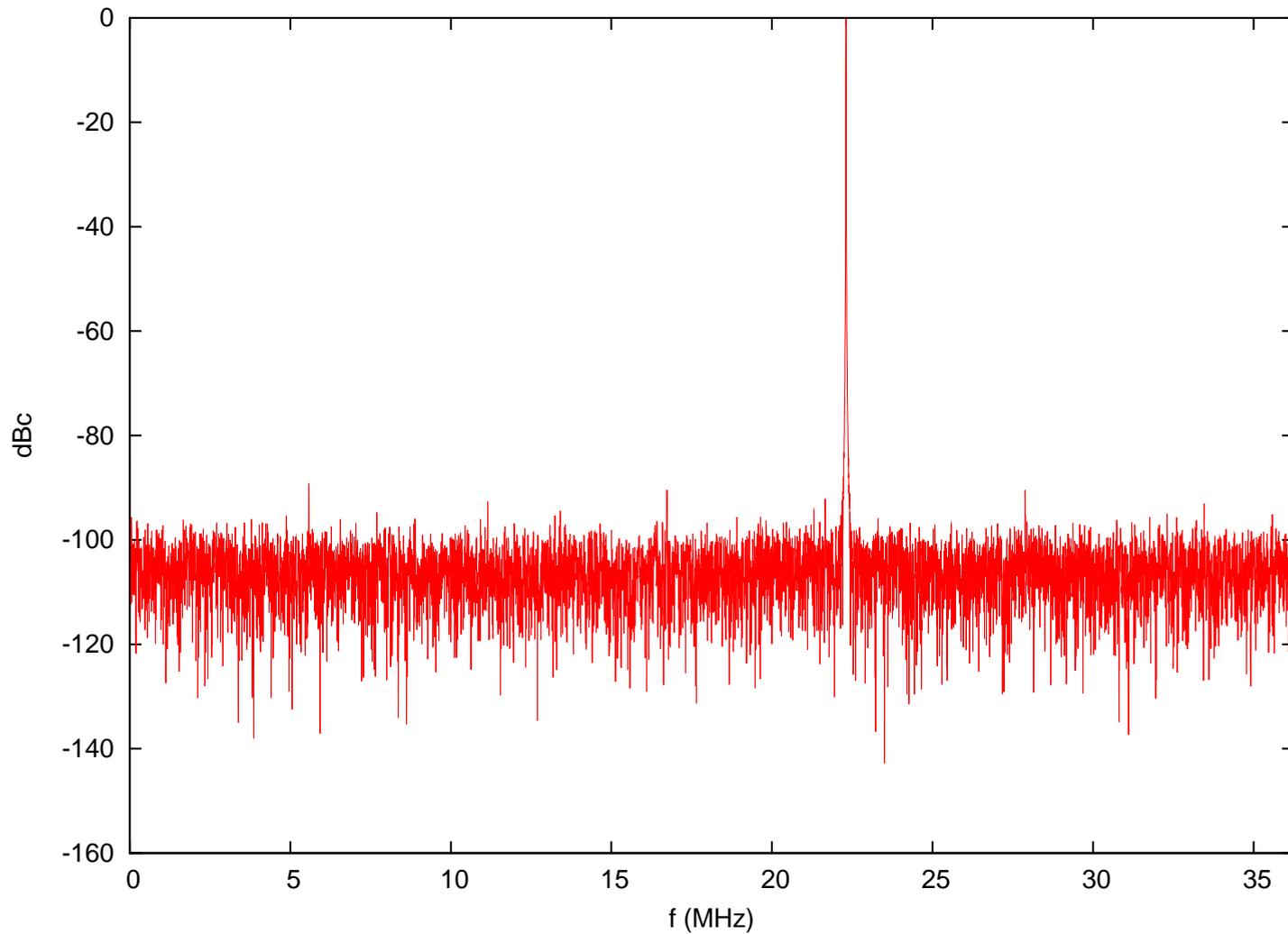
LLRF '05 (Geneva) cartoon of 14-channel two-sided 110 mm × 140 mm board. Eight needed at <\$1000 each, plus an active backplane and chassis.

## LLRF4 Board

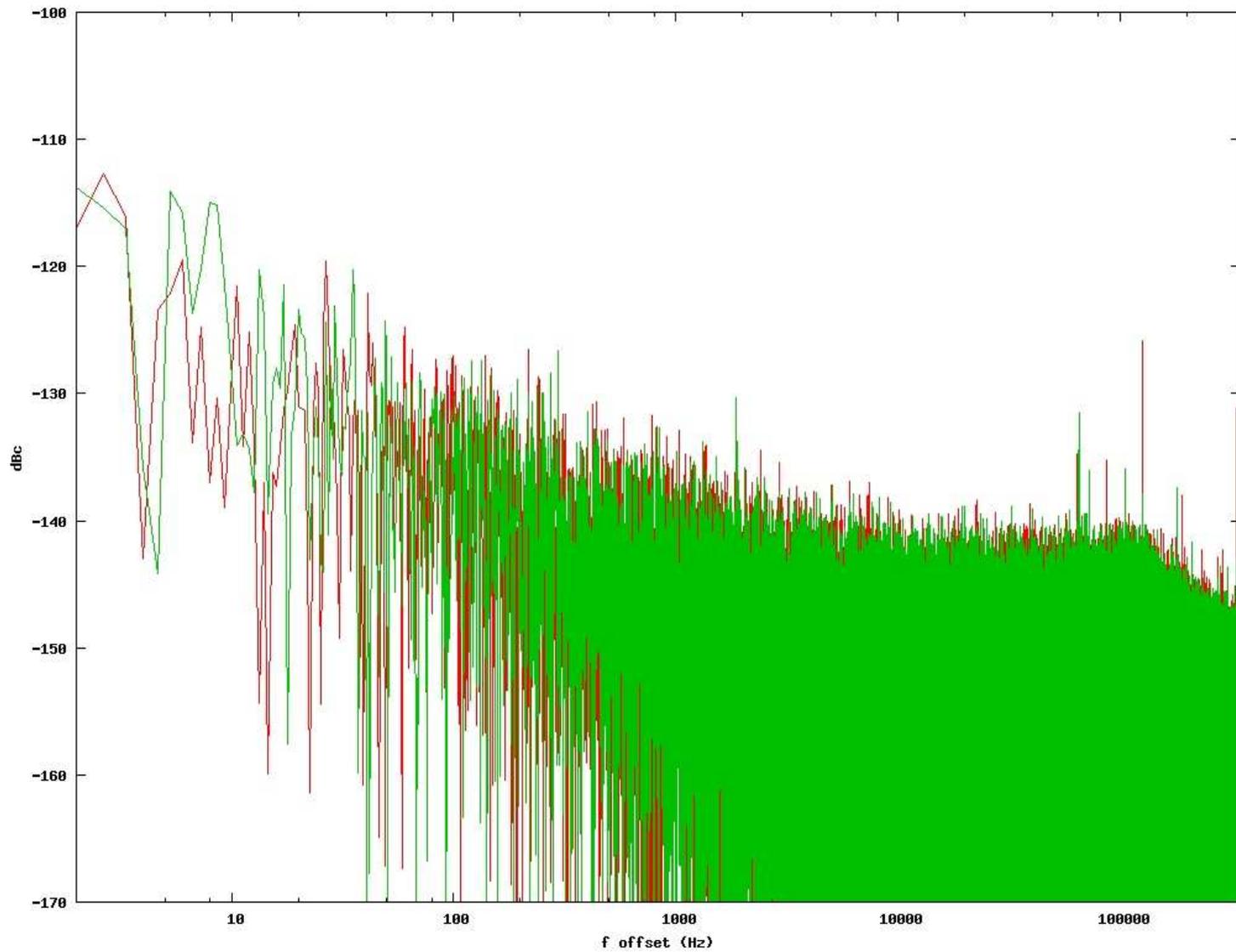
Status as of Oct 21, 2007



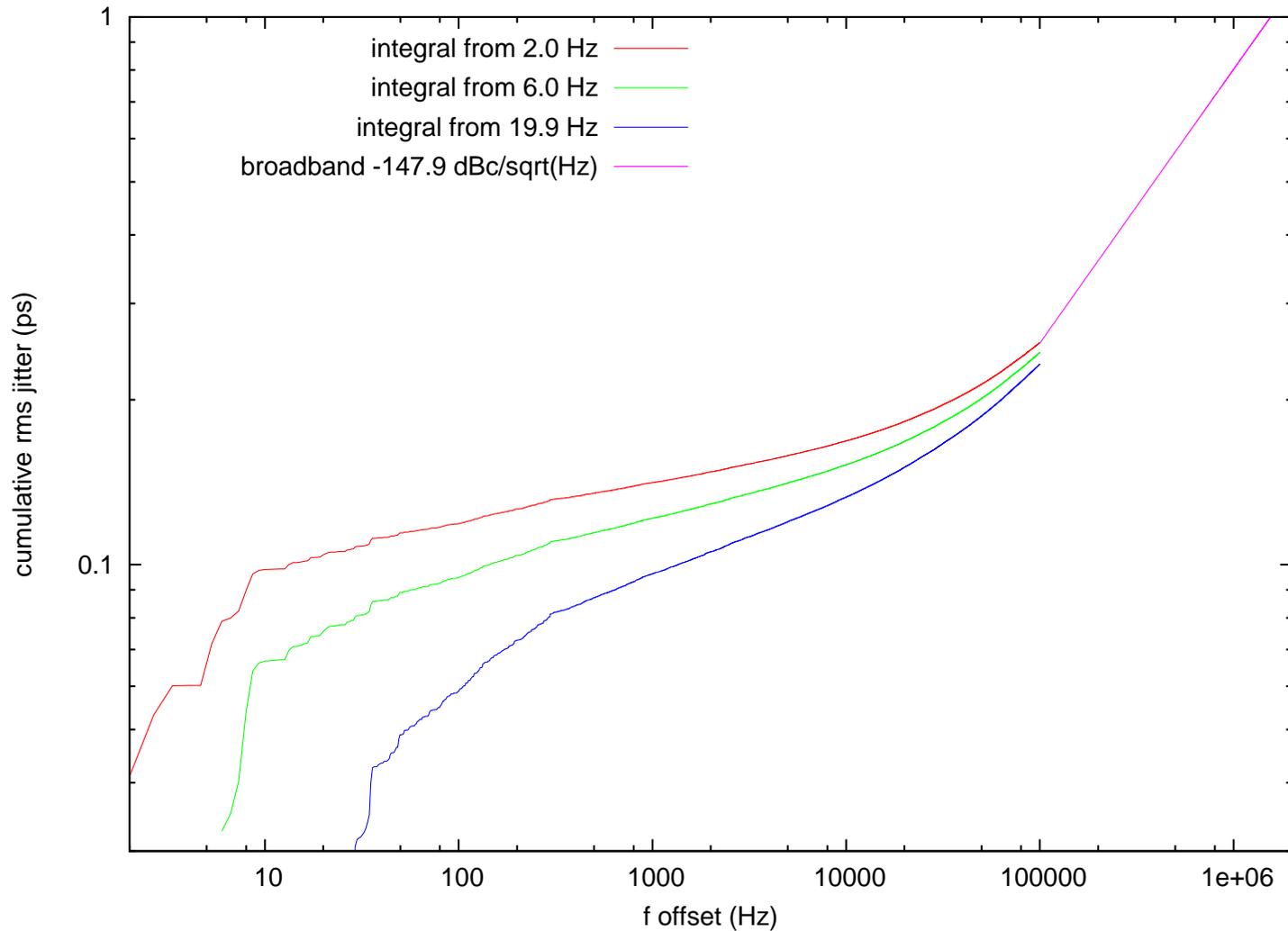
All digital and analog working (with some white wires).  
RF up/down conversion bypassed because of problems with LO distribution.  
2 boards physically at LBNL, 1 at ANL, and 3 at ORNL.  
Setting up to fabricate another batch. Order yours now!



Two boards, common clock (290 MHz), DAC output of one board routed through amplifier and filters to ADC input of second board. Single tone 9/13 of ADC clock. Largest distant spur -89 dBc 3rd harmonic (5.6 MHz).



Largest close-in spur -126 dBc at 127.4 kHz offset.  $1/f$  corner around 3 kHz: I can infer (but not prove) that noise comes from the ZFL-1000H external amplifier.



High frequency noise cutoff is normally considered the cavity closed loop bandwidth, less than 100 kHz. Low frequency cutoff based on how often the the system can digitally “autozero” to a phase reference.

# Topics for further work and discussion

- **FPGA programming:**

- Inboard cavity simulation to test communications and global controls
- Low latency inter-chip communications (LVDS on LLRF4)
- Klystron linearization

- **Hardware:**

- LO distribution and other on-board RF conversion problems
- Can we improve on the Piller/Ma phase zero scheme?
- RF connectors

- **General:**

Find a strategy to communicate with

- a commodity EPICS control computer
- the timing system

that doesn't double our engineering budget, hardware cost, and installation headaches (Ethernet/IP/UDP in FPGA fabric?)

- Design hardware that makes the software small, easy, and reliable!

- **Acknowledgements:**

- Alex Ratti, Brian Chase, Mark Champion, Hengjie Ma, Bob Dalesio, and probably half of this audience!